MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DS}	25	Vdc
Drain–Gate Voltage	V_{DG}	30	Vdc
Gate–Source Voltage*	V_{GS}	30	Vdc
Drain Current	I_D	30	mAdc
Total Device Dissipation @ $T_A = 25°C$ Derate above 25°C	P_D	300 1.7	mW mW/°C
Junction Temperature Range	T_J	175	°C
Storage Temperature Range	T_{stg}	65 to +175	°C

* Transient potentials of ± 75 Volt will not cause gate-oxide failure.

ELECTRICAL CHARACTERISTICS ($T_A = 25°C$ unless otherwise noted.)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Drain-Source Breakdown Voltage ($I_D = 10\ \mu A$, $V_{GS} = 0$)	$V_{(BR)DSX}$	25	–	Vdc
Zero-Gate-Voltage Drain Current ($V_{DS} = 10$ V, $V_{GS} = 0$) $T_A = 25°C$ $T_A = 150°C$	I_{DSS}	– –	10 10	nAdc μAdc
Gate Reverse Current ($V_{GS} = \pm 15$ Vdc, $V_{DS} = 0$)	I_{GSS}	–	± 10	pAdc
ON CHARACTERISTICS				
Gate Threshold Voltage ($V_{DS} = 10$ V, $I_D = 10\ \mu A$)	$V_{GS(Th)}$	1.0	5	Vdc
Drain-Source On-Voltage ($I_D = 2.0$ mA, $V_{GS} = 10$V)	$V_{DS(on)}$	–	1.0	V
On-State Drain Current ($V_{GS} = 10$ V, $V_{DS} = 10$ V)	$I_{D(on)}$	3.0	–	mAdc
SMALL-SIGNAL CHARACTERISTICS				
Forward Transfer Admittance ($V_{DS} = 10$ V, $I_D = 2.0$ mA, f = 1.0 kHz)	$\vert y_{fs}\vert$	1000	–	μmho
Input Capacitance ($V_{DS} = 10$ V, $V_{GS} = 0$, f = 140 kHz)	C_{iss}	–	5.0	pF
Reverse Transfer Capacitance ($V_{DS} = 0$, $V_{GS} = 0$, f = 140 kHz)	C_{rss}	–	1.3	pF
Drain-Substrate Capacitance ($V_{D(SUB)} = 10$ V, f = 140 kHz)	$C_{d(sub)}$	–	5.0	pF
Drain-Source Resistance ($V_{GS} = 10$ V, $I_D = 0$, f = 1.0 kHz)	$r_{ds(on)}$	–	300	ohms
SWITCHING CHARACTERISTICS				
Turn-On Delay (Fig. 5) — $I_D = 2.0$ mAdc, $V_{DS} = 10$ Vdc, ($V_{GS} = 10$ Vdc) (See Figure 9; Times Circuit Determined)	t_{d1}	–	45	ns
Rise Time (Fig. 6)	t_r	–	65	ns
Turn-Off Delay (Fig. 7)	t_{d2}	–	60	ns
Fall Time (Fig. 8)	t_f	–	100	ns

Figure 5.39 2N4351 Motorola *n*-channel enhancement-type MOSFET.

as $V_{GS(\text{Th})}$ and has a range of 1 to 5 V dc, depending on the unit employed. Rather than provide a range of k in Eq. (5.13), a typical level of $I_{D(\text{on})}$ (3 mA in this case) is specified at a particular level of $V_{GS(\text{on})}$ (10 V for the specified I_D level). In other words, when $V_{GS} = 10$ V, $I_D = 3$ mA. The given levels of $V_{GS(\text{Th})}$, $I_{D(\text{on})}$, and $V_{GS(\text{on})}$ permit a determination of k from Eq. (5.14) and a writing of the general equation for the transfer characteristics. The handling requirements of MOSFETs are reviewed in Section 5.9.

EXAMPLE 5.4

Using the data provided on the specification sheet of Fig. 5.39 and an average threshold voltage of $V_{GS(Th)} = 3$ V, determine:
(a) The resulting value of k for the MOSFET.
(b) The transfer characteristics.

Solution

(a) Eq. (5.14): $k = \dfrac{I_{D(on)}}{(V_{GS(on)} - V_{GS(Th)})^2}$

$$= \frac{3\text{ mA}}{(10\text{ V} - 3\text{ V})^2} = \frac{3\text{ mA}}{(7\text{ V})^2} = \frac{3 \times 10^{-3}}{49}\text{ A/V}^2$$

$$= \mathbf{0.061 \times 10^{-3}\ A/V^2}$$

(b) Eq. (5.13): $I_D = k(V_{GS} - V_T)^2$

$$= 0.061 \times 10^{-3}(V_{GS} - 3\text{ V})^2$$

For $V_{GS} = 5$ V,

$$I_D = 0.061 \times 10^{-3}(5\text{ V} - 3\text{ V})^2 = 0.061 \times 10^{-3}(2)^2$$

$$= 0.061 \times 10^{-3}(4) = 0.244\text{ mA}$$

For $V_{GS} = 8$, 10, 12, and 14 V, I_D will be 1.525, 3 (as defined), 4.94, and 7.38 mA, respectively. The transfer characteristics are sketched in Fig. 5.40.

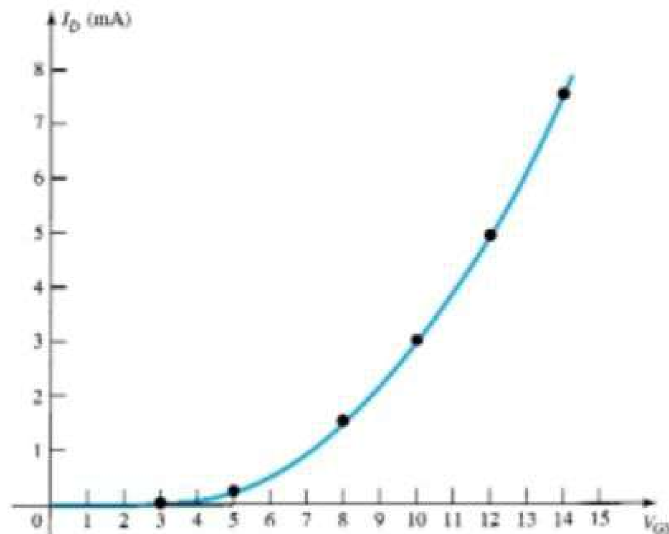

Figure 5.40 Solution to Example 5.4.

5.9 MOSFET HANDLING

The thin SiO_2 layer between the gate and channel of MOSFETs has the positive effect of providing a high-input-impedance characteristic for the device, but because of its extremely thin layer, it introduces a concern for its handling that was not present for the BJT or JFET transistors. There is often sufficient accumulation of static charge (that we pick up from our surroundings) to establish a potential difference across the thin layer that can break down the layer and establish conduction through it. It is therefore imperative that we leave the shorting (or conduction) shipping foil (or ring)